



**ANSYS**

**ONVERGENCE**  
CONFERENCES

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# SCADE定制开发分享

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**ANSYS**

# SCADE定制开发分类



SCADE模型类：  
TCP/UDP/COM/PLOT.....

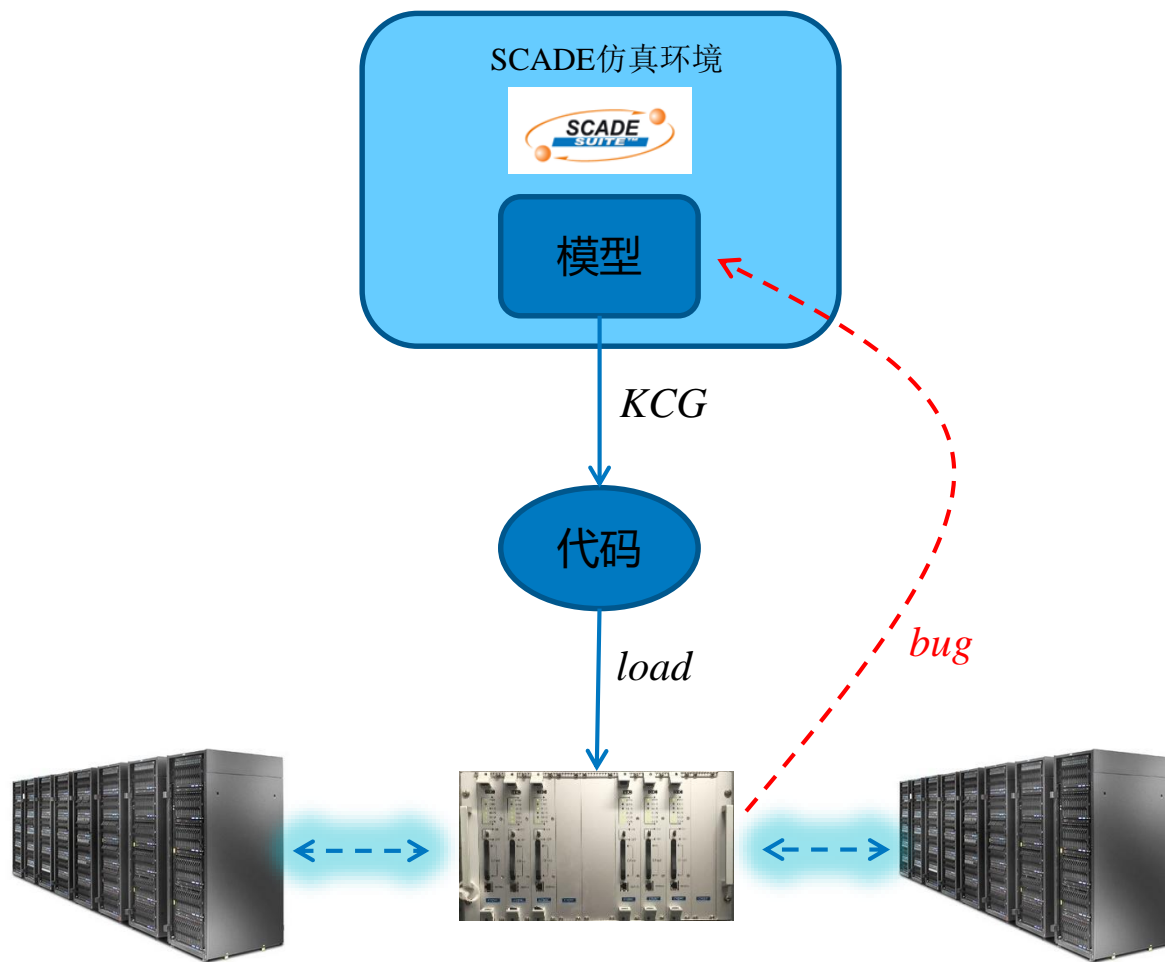
TCL脚本类：  
Document Generator/  
Simulation & Test Framework/  
Co-Simulation Platform

辅助开发类：  
SCADE Interlocking Builder

辅助验证类：  
SCADE Interpreter/  
SCADE Coder/  
SCADE Verifier/  
SCADE Test Case Generator

开发中...

# SCADE模型类：TCP/UDP/COM...



模型仿真

系统仿真

# SCADE模型类：TCP/UDP/COM...

libCommon.vsw - SCADE - Toolbox::UDP::udpRecv/diagram\_udpRecv\_1

File Edit View Operator Insert Layout Project Tools Navigate Window Help

Scade Design KCG HTML Simulation

Workspace Example::commonExample/diagram\_commonExample\_1 Toolbox::UDP::udpRecv/diagram\_udpRecv\_1 udp.c Toolbox::UDP::udpSend/diagram\_udpSend\_1

Title: UDP接收模块  
Created by: 侯锡立 M0.1  
通过parameters指定端口号和最大数据长度; 默认为本地IP, 非阻塞模式

opType #4 = 1\_ui8

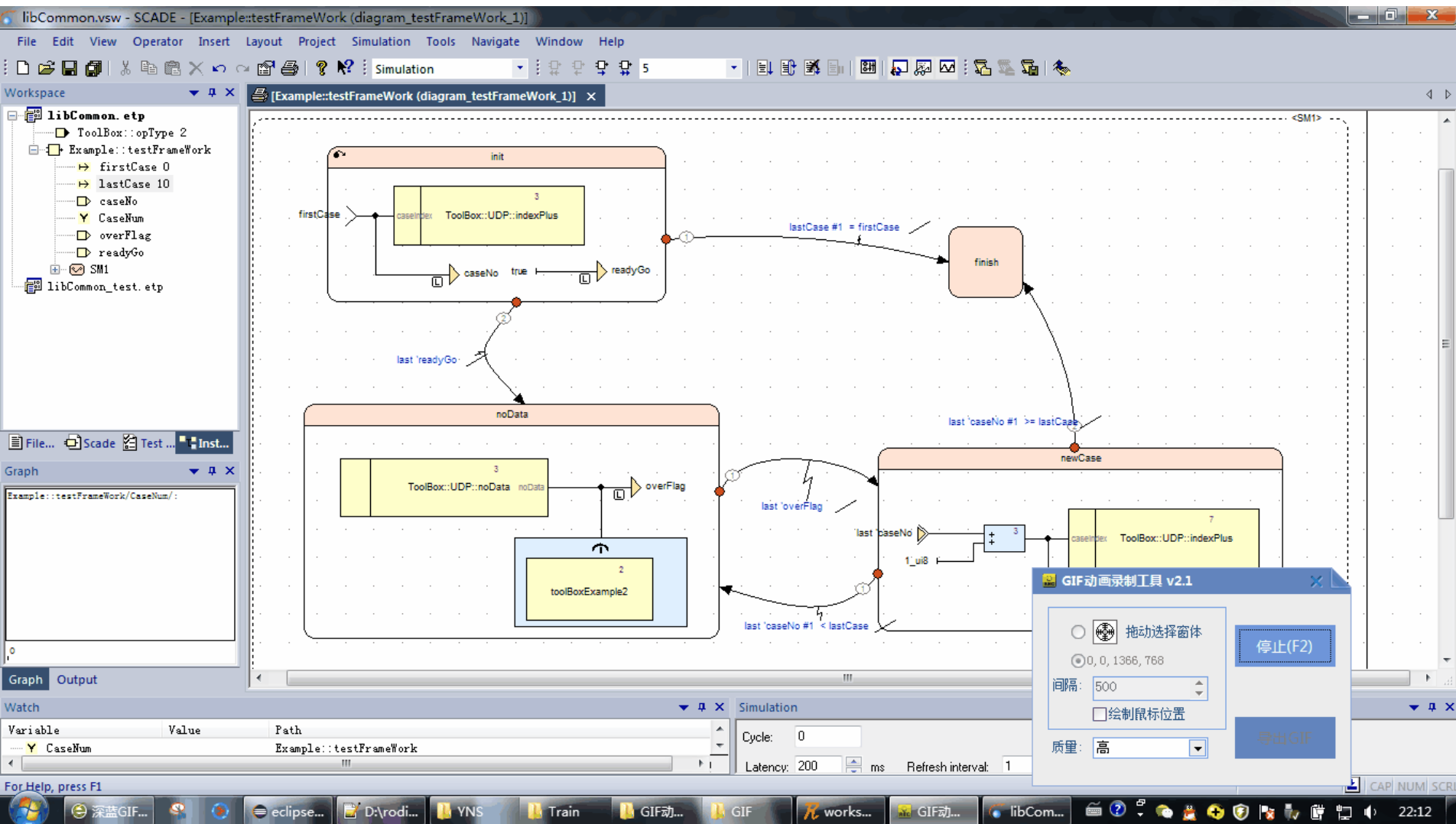
opType #3 = 2\_ui8

	A	B	C	D	E	F	G	H	I	J	K	L	M
1	length	11											
2	data	49	97	100	97	115	100	115	100	97	115	100	
3	length	11											
4	data	49	97	100	97	115	100	115	100	97	115	100	
5	length	0											
6	data												
7	length	0											
8	data												
9	length	0											
10	data												
11	length	15											
12	data	52	52	52	52	52	52	52	52	52	52	52	52

FileView Scade Test View

For Help, press F1

# SCADE模型类：TCP/UDP/COM...



The screenshot displays the SCADE software interface for a state machine model. The main workspace shows a state machine diagram with the following components:

- init state:** Contains a block 'ToolBox::UDP::indexPlus' with input 'caseNo' and output 'readyGo'. A transition labeled 'last 'readyGo'' leads to the 'noData' state.
- noData state:** Contains a block 'ToolBox::UDP::noData' with output 'overFlag'. A transition labeled 'last 'overFlag'' leads to the 'newCase' state.
- newCase state:** Contains a block 'ToolBox::UDP::indexPlus' with input 'caseNo' and output 'readyGo'. A transition labeled 'last 'caseNo #1 < lastCase'' leads to the 'noData' state. Another transition labeled 'last 'caseNo #1 >= lastCase'' leads to the 'finish' state.
- finish state:** A final state reached from 'init' via a transition labeled 'lastCase #1 = firstCase'.

The interface also includes a workspace tree on the left, a graph window, a watch table, and a simulation control panel at the bottom. A 'GIF动画录制工具 v2.1' (GIF Animation Recording Tool v2.1) window is overlaid on the bottom right, showing options for recording a GIF, including frame rate (500), quality (High), and buttons for '停止(F2)' (Stop) and '导出GIF' (Export GIF).

Variable	Value	Path
CaseNum		Example::testFrameWork

# SCADE模型类：PLOT

File Edit View Operator Insert Layout Project Simulation Tools Navigate Window Help

Simulation

Workspace

Welcome to the SCADE Product Family SAM::proOfBCCForSec/diagram\_proOfBCCForSec\_1

sc2c.log make.log [SAM::seqNumGen (seqNumGener

Constants  
Types  
Operators  
Atch4Logic  
bReadStateMachine  
convertForDataFrame <<bufSize>>  
convertForNoDataFrame <<bufSize>>  
encodeDataFrame <<bufSize>>  
encodeNoDataFrame <<bufSize>>  
factoryAcq  
factoryRSR <<bufSize>>  
factoryRSRpre  
factorySDI <<bufSize>>  
factorySDIElt1forSec <<bufSize>>  
factorySDIElt2forT  
factorySDIElt2forTadp  
factorySDIElt31  
factorySDIElt32  
factorySDIElt32  
factoryTSQ  
overTimeAndReSend  
overTimeFor3times  
proOfBCCForSec  
Interface  
IfBlock1  
diagram\_proOfBCCForSec  
proOfBCCForSecCoreElt0  
proOfBCCForSecCoreElt1A  
proOfBCCForSecCoreElt1B  
proOfBCCForSecPreElt  
proOfRSRForStation  
proOfTSDForStation  
SAMReceProcess <<bufSize>>  
SAMReceProcess4OneCom <<bufSize>>  
SAMSendProcess <<bufSize>>

mapfoldw 2 <<SAM\_RBUF\_MAX / 2>>  
index  
dataIn  
exit condition  
cmdT  
cmdZ\_H\_C

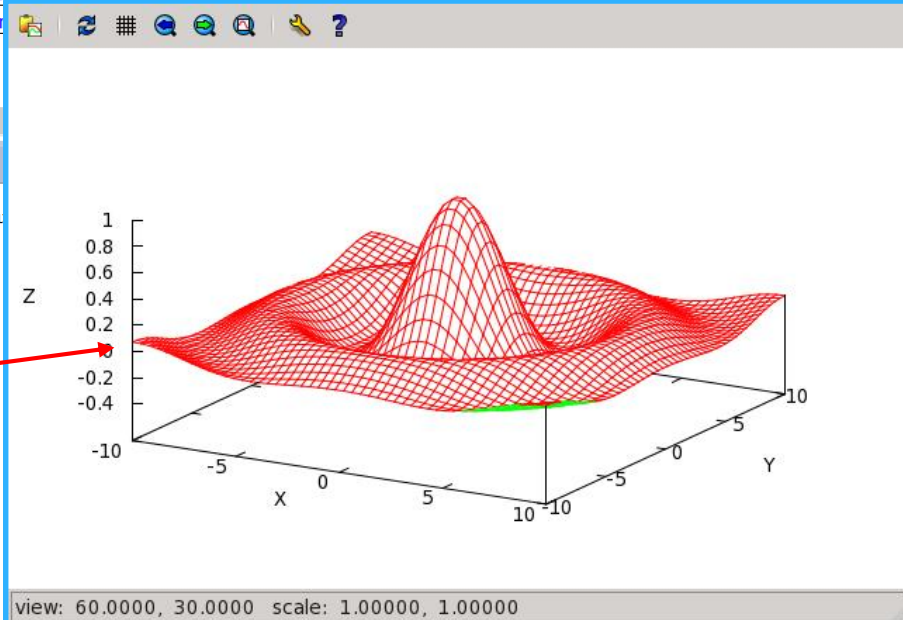
L49:uint16  
L40:frameBody\_T  
L35:bool  
L33:uint8  
L34:bool  
L30:uint16  
L29:frameBody\_T  
L31:uint32 ^ (SAM\_RBUF\_MAX / 2)  
L32:cr  
L43:uint32 ^ TwtBasicConstantsPkg::maxNumOfTwtCtrlCmd\_C  
L44:uint32  
common::msgPaste <<TwtBasicConstantsPkg::maxNumOfTwtCtrlCmd\_C, SAM\_RBUF\_MAX / 2>>  
bufferOld  
bufferNew  
length

Graph

SAM::seqNumGen/seqNumOut/: 12

SAM::seqNumGen/\_L2/: 12

Variable  
seqNumOut  
\_L2  
\_L1



view: 60.0000, 30.0000 scale: 1.00000, 1.00000

# TCL脚本类：Simulation & Test Framework



要求	仿真环境	测试环境	理想环境
各节点数据显示/检测	√	×	√
激活模块显示	√	×	√
单步/多步执行	√	×	√
断点调试	√	×	√
数据检查	×	√	√
测试结果统计	×	√	√
模型覆盖率分析	×	√	√
测试脚本管理/回归测试	×	√	√
其他数据文件读写	×	×	√
更丰富的脚本功能	√	×	√

# TCL脚本类：Simulation & Test Framework



The screenshot displays the SCADe (Simulation and Configuration Assistant Design Environment) interface. The main workspace shows a digital circuit diagram of a counter with inputs 'goon', 'reset', and 'cycleNum', and outputs 'flag' and 'count'. The circuit includes logic gates, a 4-bit counter (FBY<sup>2</sup>), and a 32-bit adder (1 ui32). A metadata box above the diagram reads: "Title: 带复位、重复计数功能的计数器" and "Created by: 侯锡立 V0.0.1".

The left sidebar shows a project tree with files like 'libCommon.etp', 'libCommon\_MTC\_INST.etp', and 'Common::counter (0/24)'. The bottom of the workspace contains a simulation control panel with 'Cycle: 0', 'Latency: 200 ms', and 'Refresh interval: 1 tick'. Below this is a table of simulation actions:

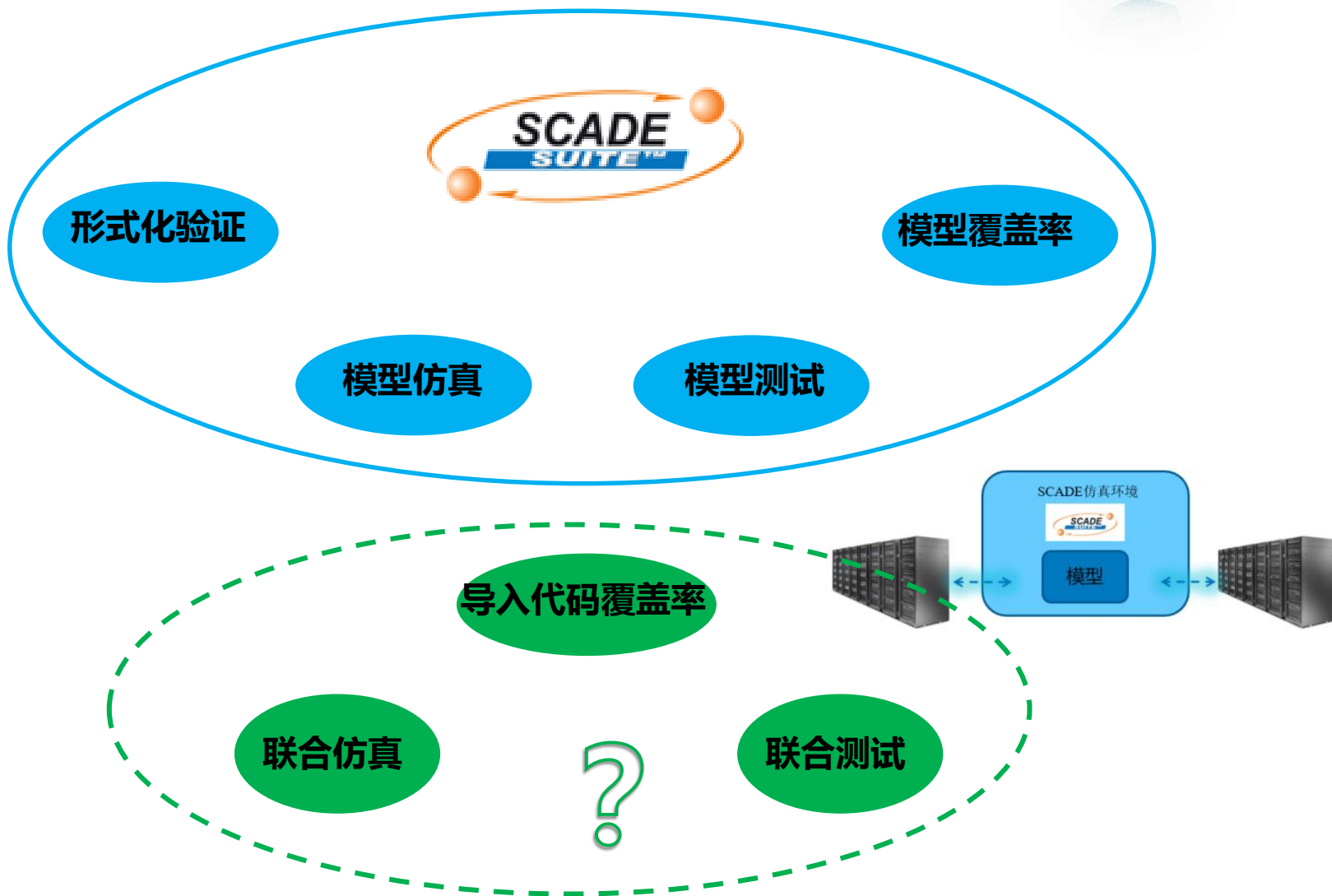
Cycle	Action
0	testEngine.sss

On the right side, there is a 'Coverage' window with three bar charts for 'Application', 'Record', and 'Gain', all showing 0% coverage. Below it is a 'Watch' window with a table of variables and their values:

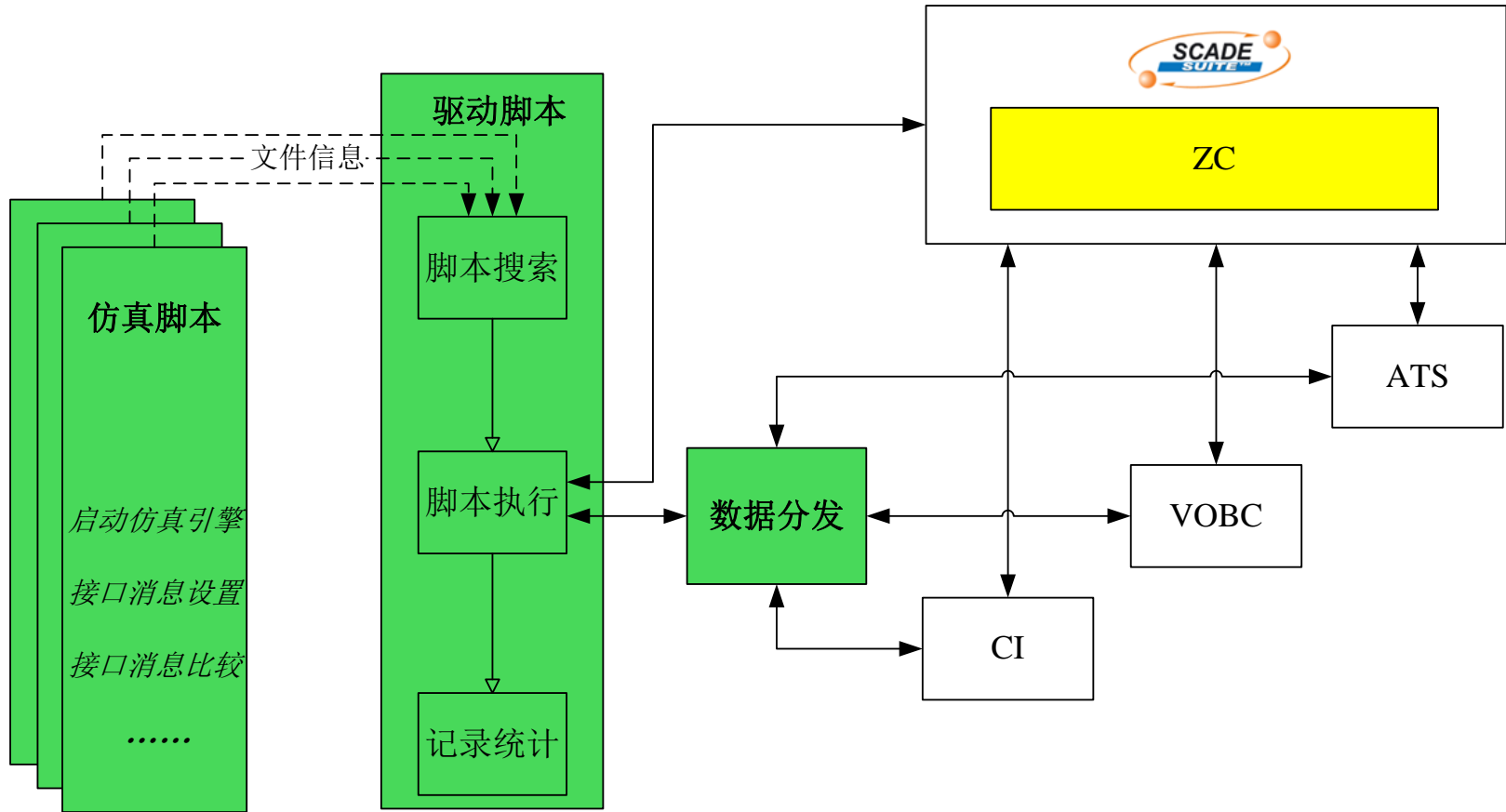
Variable	Value	Path
testResult	"\0\0\0\0"	Example::t
[0]	"\0\0\0\0"	
[1]	"\0\0\0\0"	
[2]	"\0\0\0\0"	
[3]	"\0\0\0\0"	
[4]	"\0\0\0\0"	
[5]	"\0\0\0\0"	
[6]	"\0\0\0\0"	
[7]	"\0\0\0\0"	
[8]	"\0\0\0\0"	
[9]	"\0\0\0\0"	
count	"\0\0\0\0"	Example::t



# TCL脚本类：Co-Simulation Platform



# TCL脚本类：Co-Simulation Platform



# TCL脚本类：Co-Simulation Platform



The screenshot displays the ANSYS SCADE IDE interface. The main workspace shows a testbench diagram with various components and signal connections. A green window titled "SCADE Simulator Driver V1.0" is open, showing icons for environment settings, script management, coverage, API documentation, and help. Below this, a "测试脚本列表" (Test Script List) window is visible, listing 16 test scripts. The bottom status bar shows the current project is "twMain.vsw - SCADE" and the active window is "main.aau - Debug...".

测试脚本列表	操作
D:\TWT\TWTCtrlSys\integrationTest\scripts.sim\subMain_test_01.sss	新建脚本
D:\TWT\TWTCtrlSys\integrationTest\scripts.sim\subMain_test_02.sss	运行脚本
D:\TWT\TWTCtrlSys\integrationTest\scripts.sim\subMain_test_03.sss	浏览脚本
D:\TWT\TWTCtrlSys\integrationTest\scripts.test\subMain_01.sss	删除脚本
D:\TWT\TWTCtrlSys\integrationTest\scripts.test\subMain_02.sss	调试模式
D:\TWT\TWTCtrlSys\integrationTest\scripts.test\subMain_03.sss	刷新列表
D:\TWT\TWTCtrlSys\integrationTest\scripts.test\subMain_04.sss	测试记录
D:\TWT\TWTCtrlSys\integrationTest\scripts.test\subMain_05.sss	结果统计
D:\TWT\TWTCtrlSys\integrationTest\scripts.test\subMain_06.sss	重置覆盖
D:\TWT\TWTCtrlSys\integrationTest\scripts.test\subMain_07.sss	计算覆盖
D:\TWT\TWTCtrlSys\integrationTest\scripts.test\subMain_08.sss	刷新覆盖
D:\TWT\TWTCtrlSys\integrationTest\scripts.test\subMain_09.sss	
D:\TWT\TWTCtrlSys\integrationTest\scripts.test\subMain_10.sss	
D:\TWT\TWTCtrlSys\integrationTest\scripts.test\subMain_11.sss	
D:\TWT\TWTCtrlSys\integrationTest\scripts.test\subMain_12.sss	
D:\TWT\TWTCtrlSys\integrationTest\scripts.test\subMain_13.sss	
D:\TWT\TWTCtrlSys\integrationTest\scripts.test\subMain_14.sss	
D:\TWT\TWTCtrlSys\integrationTest\scripts.test\subMain_15.sss	
D:\TWT\TWTCtrlSys\integrationTest\scripts.test\subMain_16.sss	



# TCL脚本类：Co-Simulation Platform

SCADE Simulator Driver V1.0



环境设置



脚本管理



覆盖率



API说明



关于

```
16 : : */
17 : : /*-----*/
18 : kcg_uint32 charToInt(const kcg_uint8 *psrc)
19 : {
20 :     kcg_uint32 ret = 0xFFFFFFFF;
21 :     /*- □ □ □ */
22 [+ - ]: 300120 : if (psrc)
23 :     {
24 :         ret = ((*psrc+3U)<<24U) + (*psrc+2U)<<16U) + (*psrc+1U)<<8U) + (*psrc);
25 :     }
26 :     else
27 :     {
28 :     }
29 :     return ret;
30 : }
31 :
32 :
33 : 0 : kcg_uint16 charToShort(const kcg_uint8 *psrc)
34 : {
35 :     0 : kcg_uint16 ret = 0xFFFFFFFF;
36 :     /*- □ □ □ */
37 [# # ]: 0 : if (psrc)
38 :     {
39 :         0 : ret = (*psrc+1U)<<8U) + (*psrc);
40 :     }
41 :     else
42 :     {
43 :     }
44 :     0 : return ret;
45 : }
46 :
47 :
48 : 5856 : kcg_uint8 charToChar(const kcg_uint8 *psrc)
49 : {
50 :     5856 : kcg_uint8 ret = 0xFFFFFFFF;
51 :     /*- □ □ □ */
52 [+ - ]: 5856 : if (psrc)
53 :     {
54 :         5856 : ret = (*psrc);
55 :     }
56 :     else
57 :     {
58 :     }
59 :     5856 : return ret;
60 : }
61 :
62 : routeCfgTable_T_CfgDataTypesPkg routeCfgTable_Config = {0};
63 : 122 : kcg_uint32 decomRouteCfgTable(kcg_uint8 *pFile)
64 : {
65 :     122 : kcg_uint32 i = 0 ;
```

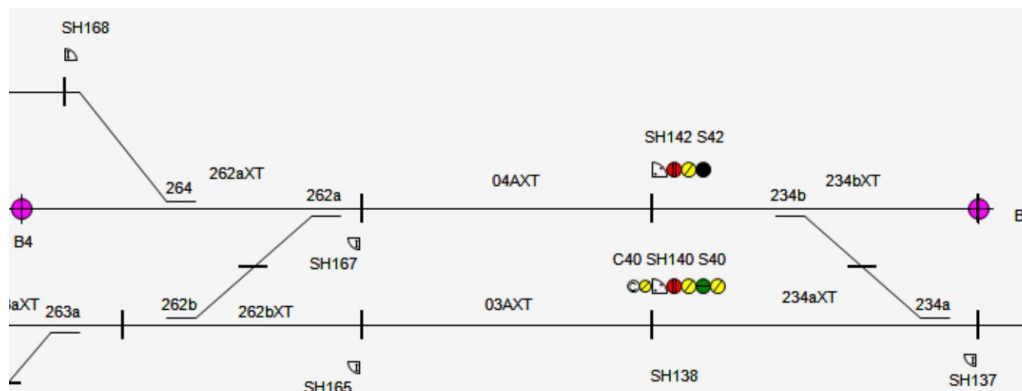
Generated by: [Debugger++ version 1.0](#)

# 辅助开发类：SCADE Interlocking Builder



- 面向对象；
- 输入站场数据/电子地图，自动生成联锁模型，测试案例，验证模型；
- 大幅压缩模型状态空间，提高形式化验证效率；

# 辅助开发类：SCADE Interlocking Builder



设计“类”模型：  
信号机模型  
道岔模型  
区段模型  
进路模型

根据站场数据/电子地图获取对象关系，  
将“类”模型实例化，并依据对象关系进行  
各对象模型接口连接

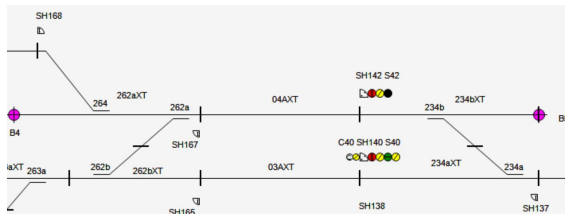
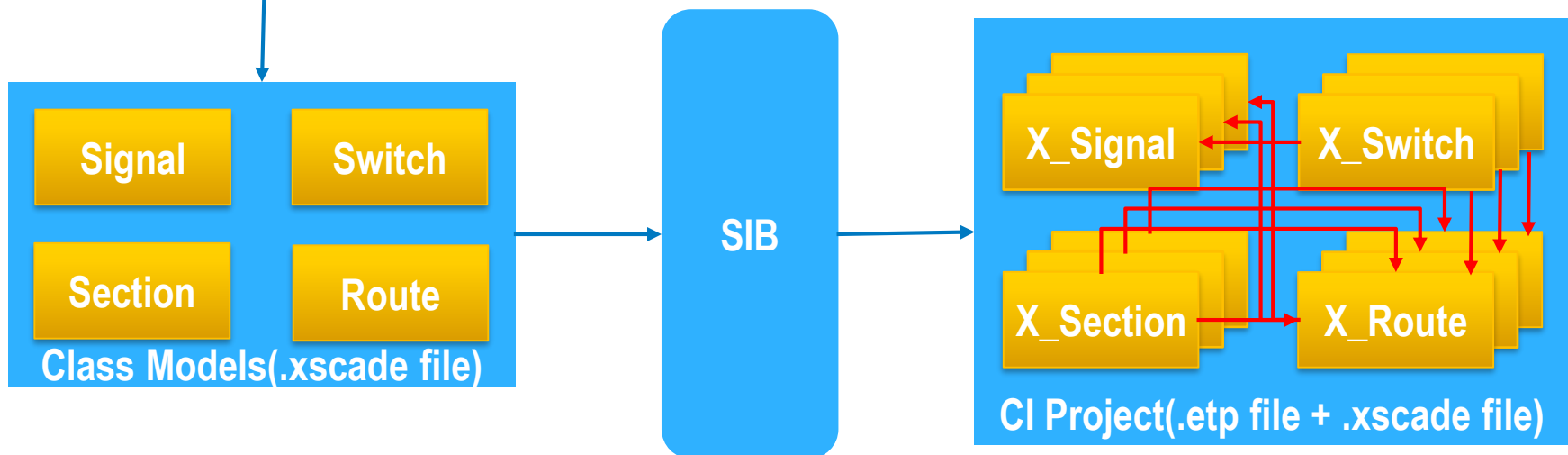
线路关系：  
信号机与进路  
进路与道岔  
进路与区段  
.....

测试“类”脚本：  
信号机测试  
道岔测试  
区段测试  
进路测试

验证“类”模型：  
安全需求  
.....

数据关系：  
允许开放  
红灯/绿灯  
搬动道岔  
区段占用

# 辅助开发类：SCADE Interlocking Builder



# 辅助开发类：SCADE Interlocking Builder



example.vsw - SCADE

File Edit View Operator Insert Layout Project Tools Navigate Window Help

Scade Design Hou Xili example.etp

Workspace

- example.etp
  - example
    - IL\_modules
    - Operators
    - ilPackage
      - Operators
        - IL\_MAIN
          - Interface
          - Locals
    - libdigital
    - liblinear
    - libmath
    - libmathext
    - libpwnlinear

Output

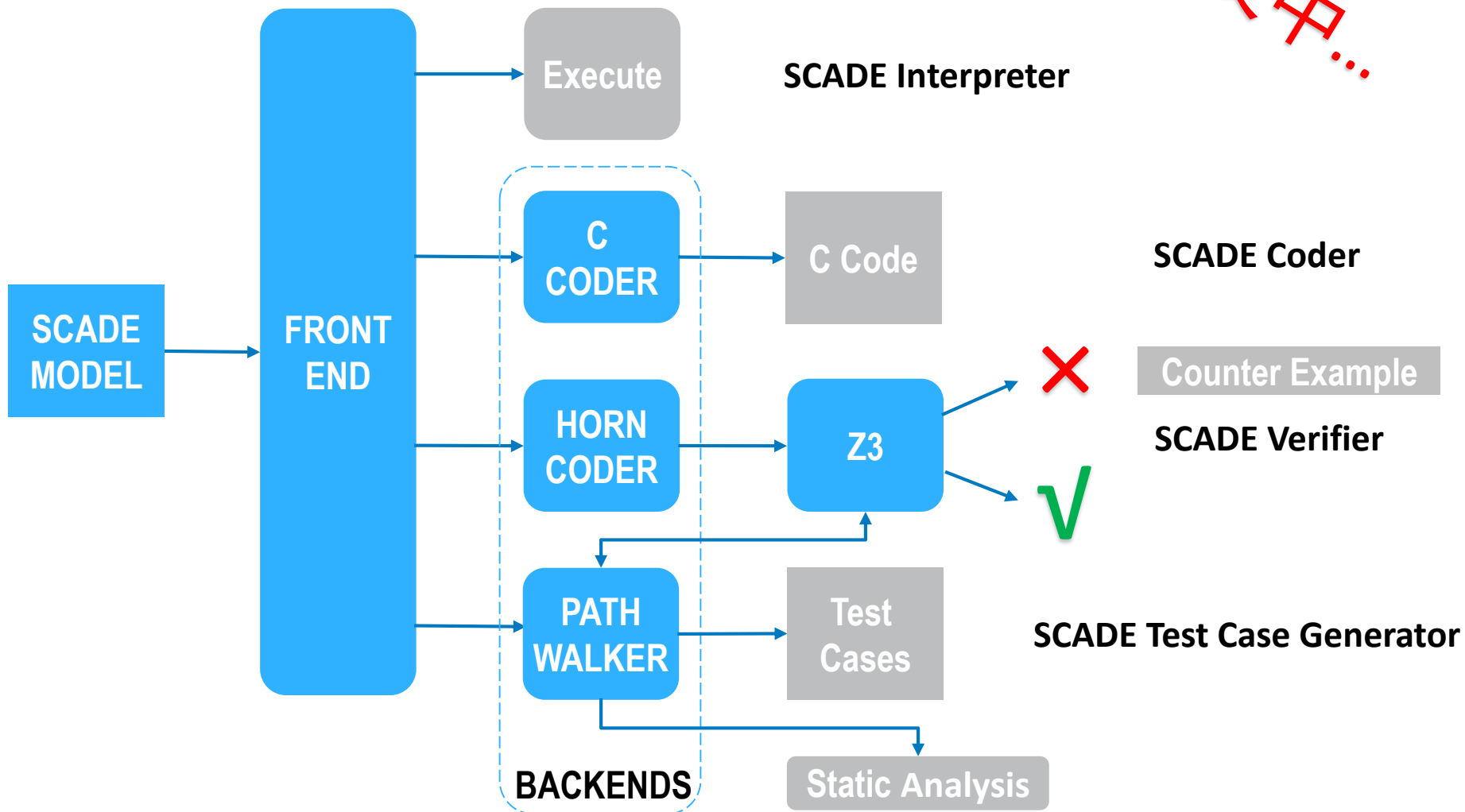
```
S_1_allow_sig_open_in : bool ^1;
S_1_keep_sig_open_in : bool ^1;
S_1_keep_sig_open_in1 : bool ^1;
S_2_allow_sig_open_in : bool ^2;
S_2_keep_sig_open_in : bool ^2;
S_2_keep_sig_open_in1 : bool ^2;
R_1_allow_sig_open : bool;
R_1_keep_sig_open : bool;
R_1_point_driver : bool;
R_2_allow_sig_open : bool;
R_2_keep_sig_open : bool;
R_2_point_driver : bool;
R_3_allow_sig_open : bool;
R_3_keep_sig_open : bool;
R_3_point_driver : bool;
SW_1_Normal_forced : bool ^1;
SW_1_Reverse_forced : bool ^1;
SW_1_srout_point : bool;
SW_2_Normal_forced : bool ^2;
SW_2_Reverse_forced : bool ^2;
SW_2_srout_point : bool;
let
  S_1_allow_sig_open_in = [R_1_allow_sig_open];
  S_1_keep_sig_open_in = [SW_1_srout_point];
  S_1_keep_sig_open_in1 = [R_1_keep_sig_open];
  S_1_HR_0, S_1_DR_0, S_1_HHR_0 = (#1 IL_modules: signal_main<1, 1, 1>>)(S_1_Signal_unblock_HMI, S_1_allow_sig_open_in, S_1_keep_sig_open_in, S_1_
  S_2_allow_sig_open_in = [R_2_allow_sig_open, R_3_allow_sig_open];
  S_2_keep_sig_open_in = [SW_1_srout_point, SW_2_srout_point];
  S_2_keep_sig_open_in1 = [R_2_keep_sig_open, R_3_keep_sig_open];
  S_2_HR_0, S_2_DR_0, S_2_HHR_0 = (#9 IL_modules: signal_main<2, 2, 2>>)(S_2_Signal_unblock_HMI, S_2_allow_sig_open_in, S_2_keep_sig_open_in, S_2_
  R_1_allow_sig_open, R_1_keep_sig_open, R_1_point_driver = #17 IL_modules: route_main(R_1_Route_Request_HMI, R_1_route_section, R_1_route_point,
  R_2_allow_sig_open, R_2_keep_sig_open, R_2_point_driver = #27 IL_modules: route_main(R_2_Route_Request_HMI, R_2_route_section, R_2_route_point,
  R_3_allow_sig_open, R_3_keep_sig_open, R_3_point_driver = #37 IL_modules: route_main(R_3_Route_Request_HMI, R_3_route_section, R_3_route_point,
  SW_1_Normal_forced = [R_1_point_driver];
  SW_1_Reverse_forced = [R_2_keep_sig_open];
  SW_1_srout_point = (#47 IL_modules: switch_main<1, 1>>)(SW_1_Normal_forced, SW_1_Reverse_forced);
  SW_2_Normal_forced = [R_2_point_driver, R_3_point_driver];
  SW_2_Reverse_forced = [R_2_keep_sig_open, R_3_keep_sig_open];
  SW_2_srout_point = (#51 IL_modules: switch_main<2, 2>>)(SW_2_Normal_forced, SW_2_Reverse_forced);
```

FileView Scade Messages Coverage Dump Build Simulator Script Matlab Info Log

For Help, press F1



# 辅助验证类：SCADE Interpreter/ Coder/Verifier/Test Case Generator

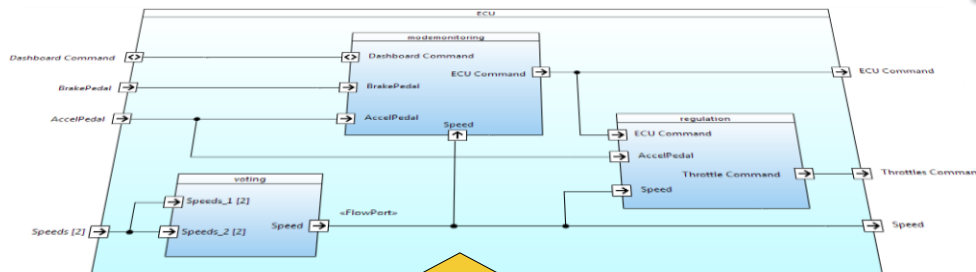


# 辅助验证类：SCADE Verifier For MBSE

开发中...



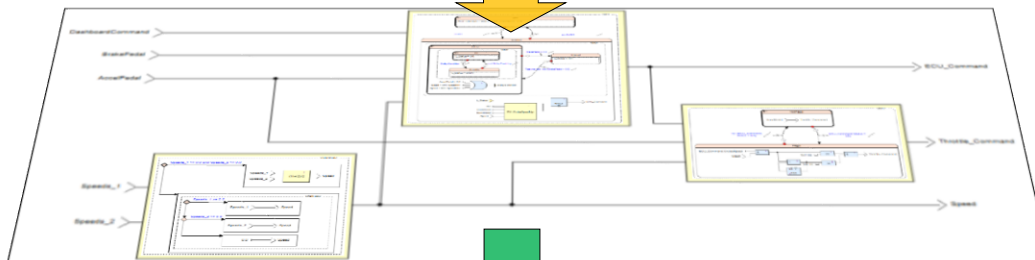
SW Architecture



Auto



SW Design



Auto



SW Coding

```

/* Architecture::Regulation */
void Regulation_Architecture(
/* ECU_Command */
tECU_cmd_Architecture *ECU_Command,
/* AccelPedal */
tPercent_Architecture AccelPedal,
/* Speed */
tVehicleSpeed_Architecture Speed, outC_Regulation_Architecture *outC)
{
    kcg_float32 tmp;
    /* SMI:Regul_L3 */
    kcg_float32 _L3_Regul_SMI;
    /* SMI */
    SSM_ST_SMI SM1_state_act;
    /* SMI */
    kcg_bool SM1_reset_act;
    /* SMI */
    switch (outC->SM1_state_nxt) {
    case SSM_st_NotRegul_SMI :
        SM1_reset_act = (*ECU_Command).Status == ON_Architecture;
        if (SM1_reset_act) {
            SM1_state_act = SSM_st_Regul_SMI;
        }
    else {
        SM1_state_act = SSM_st_NotRegul_SMI;
    }
    }
    break;
}
    
```

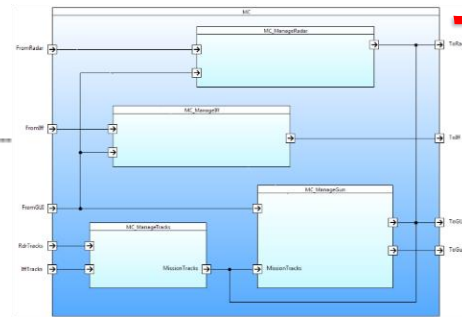
C

# 辅助验证类：SCADE Verifier For MBSE

开发中...



```
Contracts:
Assume: <expr>;
Guarantee: <expr>;
--%PROPERTY ["<name>"] <bool_expr>;
```



SCADE Interlocking Builder

Auto

```
✓ assume_ID: expr
✓ guarantee_ID: expr
```

Observer → bool



SCADE MODEL

FRONT END

HORN CODER

Z3

✗

Counter Example

SCADE Verifier

✓

# 感谢聆听！



ANSYS

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